

European Library-based flow

Embedded Silicon test Instruments

ELESIS final review December 2015

D4 Systems

UNIVERSITY OF TWENTE.

Goal & Technology Goal: Tools to support methods for qualifying dependability sensors IP in System-On-Chip Method: New software comprising a model driven, statistical simulation approach with build-in dependability IP database. A tool to assess the quality and sustained performance of SoC's over operational lifetime **Dependability Model Simulator - DMS** ELESIS exploitation & KPI's: connecting project targets to customer key benefits with new DMS tool ELESIS KPI DMS: customer key benefit Market value of D4T DMS tool Reduced EDA integration time for dependability features. ТІМЕ 100% Cost reduction of Advanced sensor-in-SoC capability analysis due to accurate model database QUALITY 90% (normalized) 58% per design Reduced "what-if" simulation effort for dependability IP in SoC TIME 80% 70% Reduced wafer and silicon waste by more efficient IP debug COST Si scrap 60% ODM/IP chip integrator cost 50% EDA simulation Purchase/integrate dependability IP instrument Dependability IP selection Schematics capability analysis **ELESIS design** design & netlist 40% ↓ chir Г 30% EDA integration sim OK? 20% output 10% D4T Systems DMS tool 0% IP providers Foundry is positioned at the pre-D4 Systems wo/D4T DMS w/ D4T DMS silicon design phase DMS software manufacturing "What-if"__ ELESIS IP Testing FLESIS testina Sensor-in-SoC instruments & sensors performance model database Packaging analysis ELESIS technology results: DMS software demonstration of dependability IP evaluation on AMS DUT From transistor level circuit simulation to Model based design with statistical analysis Dependability Model Simulator demo: Ichip DC offset sensor Vir Capability analysis on ELESIS sensor to ational settings Vin1 Vin2 monitor DC drift due to aging in SoC IP. measure variables Response variables DCout(V) Vin1(V) This dependability IP is evaluated on two Observe Vin2(V) parameter for devices with DMS: pass /fail 1) General purpose OpAmp IP block for SoC's 2) High grade, robust OpAmp IP for SerDes ↑ high speed communication. ه گ ک Accuracy Bits resolution Model parameters: curacy Defined by technology noise Design set-points IEEE P1687 con nd design (consta Defined by user in test configuration (variable Dependability sensor: Design set-points Min/max settin 1) DC offset drift due to NBTI. IP model database 2) DC offset sensed from AC signals through gain optimized loop III DIB model 📢 Test platform 🕂 Test List 😼 Databases Workbench: sensor test and simulation setup Analysis: capability of dependability IP in SoC e of available dat Database with libraries. The ELESIS instruments a ents are implemented for two variants ELESTS DC offse ffset C65 single ck 💌 Global Test Language (V)duoo The datasheet parameters (Meab) as they will be used in the sensor model Offset pred Aging prediction \$00 \$00 \$00 \$00 \$00 Input Add DTI Delete 100 DMS analysis output Detected DC drift is displayed with statistical boundaries. Obser DUT DC offset =>

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