European Library-based flow of Embedded Silicon Test Instruments

ELESIS final review
December 2015

D4T Systems

Goal & Technology

Goal: Test Access Standardization of Embedded Test Instruments and protocol automation
Method: High-speed serial test interface with LVDS and serialization

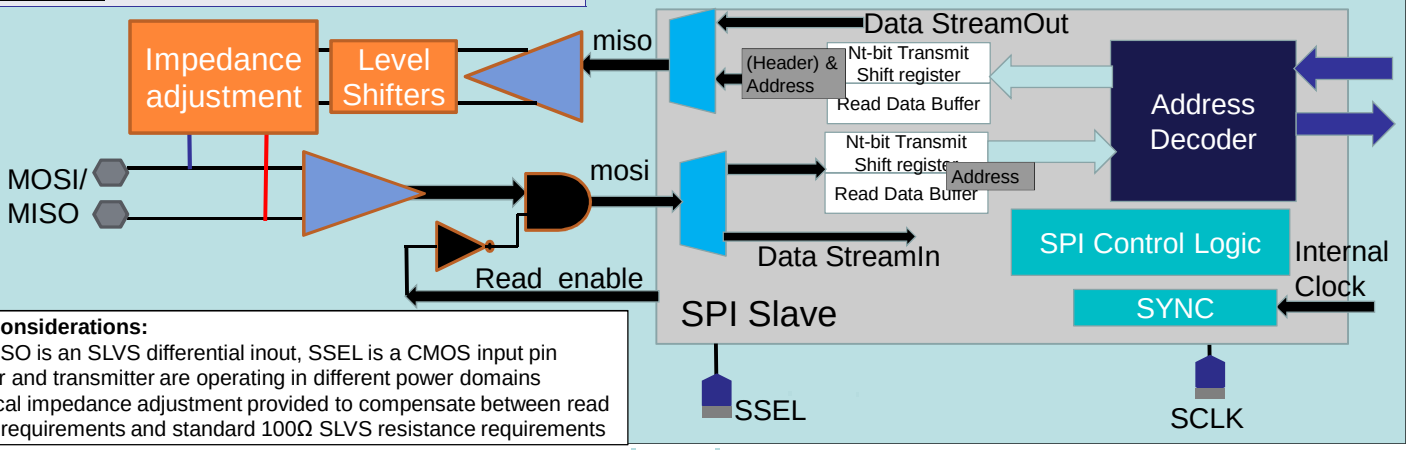
New test architecture for streaming and distributing test data with high bandwidth and low pin count

Test Access Standardization of ETI: High-Speed Link

ELESIS KPI's

Key benefits	ELESIS KPI
Test Interface Standardization	QUALITY
Test development protocol automation	TIME
Test Pin reduction	COST

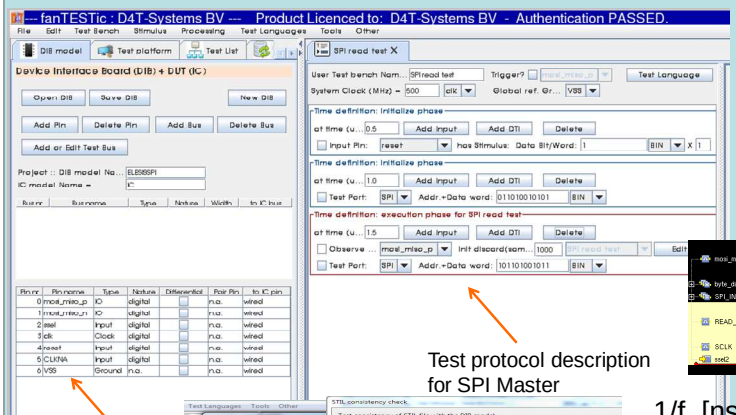
SPI Extension to enable higher operating frequencies



Design Considerations:
•MOSI/MISO is an SLVS differential inout, SSEL is a CMOS input pin
• Receiver and transmitter are operating in different power domains
• Dynamical impedance adjustment provided to compensate between read and write requirements and standard 100Ω SLVS resistance requirements

ELESIS technology results: Crucial Design Achievements, Test Protocol Automation

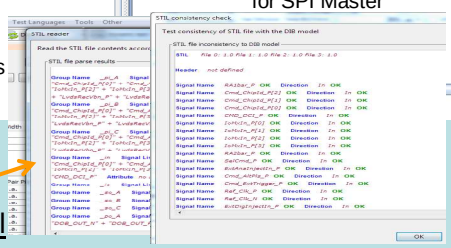
Automatic Test Protocol Generation with D4T Systems fanTESTic tool



Test protocol description for SPI Master

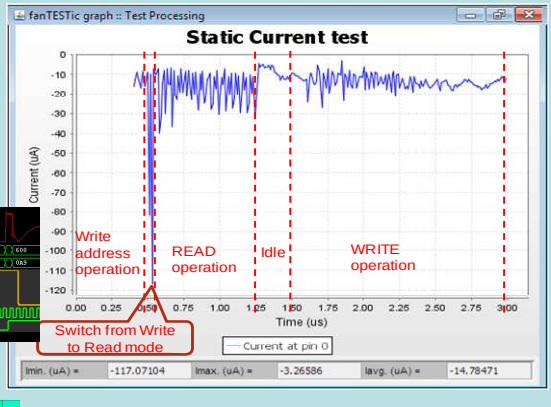
Primary ports

STIL Protocol Generation

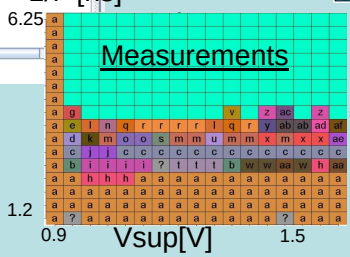


Simulation Testbench Generation

Analysis: Current and Power Measurement



Measurements



High Speed test link - final achievements:
Max Speed <= 300 MHz
Pincount <= 3
Power (static) =16.8µW
Power(dynamic) = 17.736µW
Area = 17600 µm^2
BER < 1x10^{-12} @300MHz

ECSEL Joint Undertaking
Electronic Components and Systems for European Leadership

For product pricing, services and technical information, please contact:
Email: info@d4t-systems.com
More info: www.d4t-systems.com and www.elesis.eu